WHAT IS CLAIMED IS:

1. A method, comprising:

retrieving an instruction from a memory unit;

pre-decoding the instruction at a direct memory access unit; and

providing the pre-decoded instruction from the direct memory access unit to a processing element.

2. The method of claim 1, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element.

3. The method of claim 2, wherein the pre-decoded instruction is a completely decoded instruction to be executed by the processing element.

4. The method of claim 1, further comprising:

decoding the pre-decoded instruction at the processing element; and

executing the decoded instruction via a processor pipeline.

5. The method of claim 1, further comprising:

loading instructions into the memory unit during a boot-up process.

6. The method of claim 1, wherein the processing element is a reduced instruction set computer device.

7. The method of claim 6, wherein the pre-decoded instruction comprises execution control signals.

8. An apparatus, comprising:

an input path to receive an instruction from a memory unit;

a direct memory access unit including an instruction pre-decoder to pre-decode the instruction; and

an output path to provide a pre-decoded instruction from the direct memory access unit to a processing element.

9. The apparatus of claim 8, further comprising:

the memory unit coupled to the input path.

10. The apparatus of claim 9, further comprising:

the processing element coupled to the output path.

11. The apparatus of claim 10, wherein the processing element includes a local memory to store the pre-decoded instruction.

12. The apparatus of claim 10, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder.

13. The apparatus of claim 10, wherein the input path has n bits, the output path has q bits, and $n < q$.

14. The apparatus of claim 10, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit.

15. The apparatus of claim 10, wherein the processing element is a reduced instruction set computer device having an instruction pipeline.

16. An article, comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

retrieving an instruction from a memory unit,

pre-decoding the instruction at a direct memory access unit, and

providing the pre-decoded instruction from the direct memory access unit to a processing element.

17. The article of claim 16, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element.

18. An apparatus, including:

a global memory to store instructions;

an instruction pre-decoder; and

a processor, wherein the instruction pre-decoder is to pre-decode an instruction as it is being transferred from the global memory to the processor.

19. The apparatus of claim 18, further comprising:

a direct memory access unit to arrange for the instruction to be retrieved from the global memory unit and to arrange for a pre-decoded instruction to be provided to the processor.

20. The apparatus of claim 18, wherein a pre-decoded instruction comprises execution control signals.

21. A system, comprising:

a multi-directional antenna; and

an apparatus having a direct memory access unit that includes:

an input path to receive an instruction from a memory unit,

an instruction pre-decoder to pre-decode the instruction, and

an output path to provide a pre-decoded instruction to a processing element.

22. The system of claim 21, wherein the apparatus is a digital base band processor.

23. The system of claim 22, wherein the digital base band processor is formed as a system on a chip.

24. The system of claim 21, wherein the system is a code-division multiple access base station.